Future Technology Devices International Ltd.

FT245R USB FIFO I.C.

Incorporating FTDIChip-ID™ Security Dongle

The **FT245R** *is the latest device to be added to FTDI's range of USB FIFO interface Integrated Circuit Devices. The FT245R is a USB to parallel FIFO interface, with the new FTDIChip-ID™ security dongle feature. In addition, asynchronous and synchronous bit bang interface modes are available. USB to parallel designs using the FT245R have been further simplified by fully integrating the external EEPROM, clock circuit and USB resistors onto the device.*

The FT245R adds a new function compared with its predecessors, effectively making it a "2-in-1" chip for some application areas. A unique number (the FTDIChip-ID™) is burnt into the device during manufacture and is readable over USB, thus forming the basis of a security dongle which can be used to protect customer application software from being copied.

The FT245R is available in Pb-free (RoHS compliant) compact 28-Lead SSOP and QFN-32 packages.

1. Features

1.1 Hardware Features

- Single chip USB to parallel FIFO bidirectional data transfer interface.
- Entire USB protocol handled on the chip - No USB-specific firmware programming required.
- Simple interface to MCU / PLD / FPGA logic with simple 4-wire handshake interface.
- Data transfer rate to 1 Megabyte / second - D2XX Direct Drivers.
- Data transfer rate to 300 kilobyte / second - VCP Drivers.
- 256 byte receive buffer and 128 byte transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- FTDI's royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.
- New USB FTDIChip-ID™ feature.
- FIFO receive and transmit buffers for high data throughput.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD# and WR# strobes allow the data bus to be used as a general purpose I/O port.
- Integrated 1024 Bit internal EEPROM for storing USB VID, PID, serial number and product description strings.
- Device supplied preprogrammed with unique USB serial number.
- Support for USB suspend / resume through PWREN# pin and Wake Up pin function.
- In-built support for event characters.
- Support for bus powered, self powered, and high-power bus powered USB configurations.
- Integrated 3.3V level converter for USB I/O .
- Integrated level converter on FIFO interface and control pins for interfacing to 5V - 1.8V Logic.
- True 5V / 3.3V / 2.8V / 1.8V CMOS drive output and TTL input.
- High I/O pin output drive option.
- Integrated USB resistors.
- Integrated power-on-reset circuit.
- Fully integrated clock - no external crystal, oscillator, or resonator required.
- Fully integrated AVCC supply filtering - No separate AVCC pin and no external R-C filter required.
- USB bulk transfer mode.
- 3.3V to 5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI / OHCI / EHCI host controller compatible
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 28 Pin SSOP and QFN-32 packages (both RoHS compliant).

1.2 Driver Support

Royalty-Free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 98, 98SE, ME, 2000, Server 2003, XP.
- Windows Vista / Longhorn*
- Windows XP 64-bit.*
- Windows XP Embedded.
- Windows CE.NET 4.2 & 5.0
- MAC OS 8 / 9, OS-X
- Linux 2.4 and greater

Royalty-Free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 98, 98SE, ME, 2000, Server 2003, XP.
- Windows Vista / Longhorn*
- Windows XP 64-bit.*
- Windows XP Embedded.
- Windows CE.NET 4.2 & 5.0
- Linux 2.4 and greater

The drivers listed above are all available to download for free from the FTDI website. Various 3rd Party Drivers are also available for various other operating systems - see the FTDI website for details.

* Currently Under Development. Contact FTDI for availability.

1.3 Typical Applications

- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU / PLD / FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software / Hardware Encryption Dongles

2. Enhancements

2.1 Device Enhancements and Key Features

This section summarises the enhancements and the key features of the FT245R device. For further details, consult the device pin-out description and functional description sections.

Integrated Clock Circuit - Previous generations of FTDI's USB to parallel FIFO interface devices required an external crystal or ceramic resonator. The clock circuit has now been integrated onto the device meaning that no crystal or ceramic resonator is required. However, if required, an external 12MHz crystal can be used as the clock source.

Integrated EEPROM - Previous generations of FTDI's USB to parallel FIFO interface devices required an external EEPROM if the device were to use USB Vendor ID (VID), Product ID (PID), serial number and product description strings other than the default values in the device itself. This external EEPROM has now been integrated onto the FT245R chip meaning that all designs have the option to change the product description strings. A user area of the internal EEPROM is available for storing additional data. The internal EEPROM is programmable in circuit, over USB without any additional voltage requirement.

Preprogrammed EEPROM - The FT245R is supplied with its internal EEPROM preprogrammed with a serial number which is unique to each individual device. This, in most cases, will remove the need to program the device EEPROM.

Integrated USB Resistors - Previous generations of FTDI's USB to parallel FIFO interface devices required two external series resistors on the USBDP and USBDM lines, and a 1.5 kΩ pull up resistor on USBDP. These three resistors have now been integrated onto the device.

Integrated AVCC Filtering - Previous generations of FTDI's USB to parallel FIFO interface devices had a separate AVCC pin - the supply to the internal PLL. This pin required an external R-C filter. The separate AVCC pin is now connected internally to VCC, and the filter has now been integrated onto the chip.

Less External Components - Integration of the crystal, EEPROM, USB resistors, and AVCC filter will substantially reduce the bill of materials cost for USB interface designs using the FT245R compared to its FT245BM predecessor.

Transmit and Receive Buffer Smoothing - The FT245R's 256 byte receive buffer and 128 byte transmit buffer utilise new buffer smoothing technology to allow for high data throughput.

Enhanced Asynchronous Bit Bang Mode with RD# and WR# Strobes - The FT245R supports FTDI's BM chip bit bang mode. In bit bang mode, the eight parallel FIFO data bus lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the FT245R device this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the bit bang I/O bus. This option will be described more fully in a separate application note

Synchronous Bit Bang Mode - Synchronous bit bang mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. Thus making it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. The feature was previously seen in FTDI's FT2232C device. This option will be described more fully in a separate application note.

Lower Supply Voltage - Previous generations of the chip required 5V supply on the VCC pin. The FT245R will work with a Vcc supply in the range 3.3V - 5V. Bus powered designs would still take their supply from the 5V on the USB bus, but for self powered designs where only 3.3V is available, and there is no 5V supply, there is no longer any need for an additional external regulator.

Integrated Level Converter on FIFO Interface and Control Signals - VCCIO pin supply can be from 1.8V to 5V. Connecting the VCCIO pin to 1.8V, 2.8V, or 3.3V allows the device to directly interface to 1.8V, 2.8V or 3.3V and other logic families without the need for external level converter I.C.s

5V / 3.3V / 2.8V / 1.8V Logic Interface - The FT245R provides *true* CMOS Drive Outputs and TTL level Inputs.

Integrated Power-On-Reset (POR) Circuit- The device incorporates an internal POR function. A RESET# pin is available in order to allow external logic to reset the FT245R where required. However, for many applications the RESET# pin can be left unconnected, or pulled up to VCCIO.

Wake Up Function - If USB is in suspend mode, and remote wake up has been enabled in the internal EEPROM (it is enabled by default), the RXF# pin becomes an input. Strobing this pin low will cause the FT245R to request a resume from suspend on the USB bus. Normally this can be used to wake up the host PC from suspend

Lower Operating and Suspend Current - The device operating supply current has been further reduced to 15mA, and the suspend current has been reduced to around 70µA. This allows a greater margin for peripherals to meet the USB suspend current limit of 500µA.

Low USB Bandwidth Consumption - The operation of the USB interface to the FT245R has been designed to use as little as possible of the total USB bandwidth available from the USB host controller.

High Output Drive Option - The parallel FIFO interface and the four FIFO handshake pins can be made to drive out at three times the standard signal drive level thus allowing multiple devices to be driven, or devices that require a greater signal drive strength to be interfaced to the FT245R. This option is configured in the internal EEPROM.

Power Management Control for USB Bus Powered, High Current Designs- The PWREN# signal can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. An option in the internal EEPROM makes the device gently pull down on its FIFO interface lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

FTDIChip-ID™ - Each FT245R is assigned a unique number which is burnt into the device at manufacture. This ID number cannot be reprogrammed by product manufacturers or end-users. This allows the possibility of using FT245R based dongles for software licensing. Further to this, a renewable license scheme can be implemented based on the FTDIChip-ID™ number when encrypted with other information. This encrypted number can be stored in the user area of the FT245R internal EEPROM, and can be decrypted, then compared with the protected FTDIChip-ID™ to verify that a license is valid. Web based applications can be used to maintain product licensing this way. An application note describing this feature is available separately from the FTDI website.

Improved EMI Performance - The reduced operating current and improved on-chip VCC decoupling significantly improves the ease of PCB design requirements in order to meet FCC, CE and other EMI related specifications.

Programmable FIFO TX Buffer Timeout - The FIFO TX buffer timeout is used to flush remaining data from the receive buffer. This timeout defaults to 16ms, but is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be optimised for protocols that require fast response times from short data packets.

Extended Operating Temperature Range - The FT232R operates over an extended temperature range of -40º to +85º C thus allowing the device to be used in automotive and industrial applications.

New Package Options - The FT245R is available in two packages - a compact 28 pin SSOP (**FT245RL**) and an ultra-compact 5mm x 5mm pinless QFN-32 package (**FT245RQ**). Both packages are lead (Pb) free, and use a 'green' compound. Both packages are fully compliant with European Union directive 2002/95/EC.

3. Block Diagram

3.1 Block Diagram (Simplified)

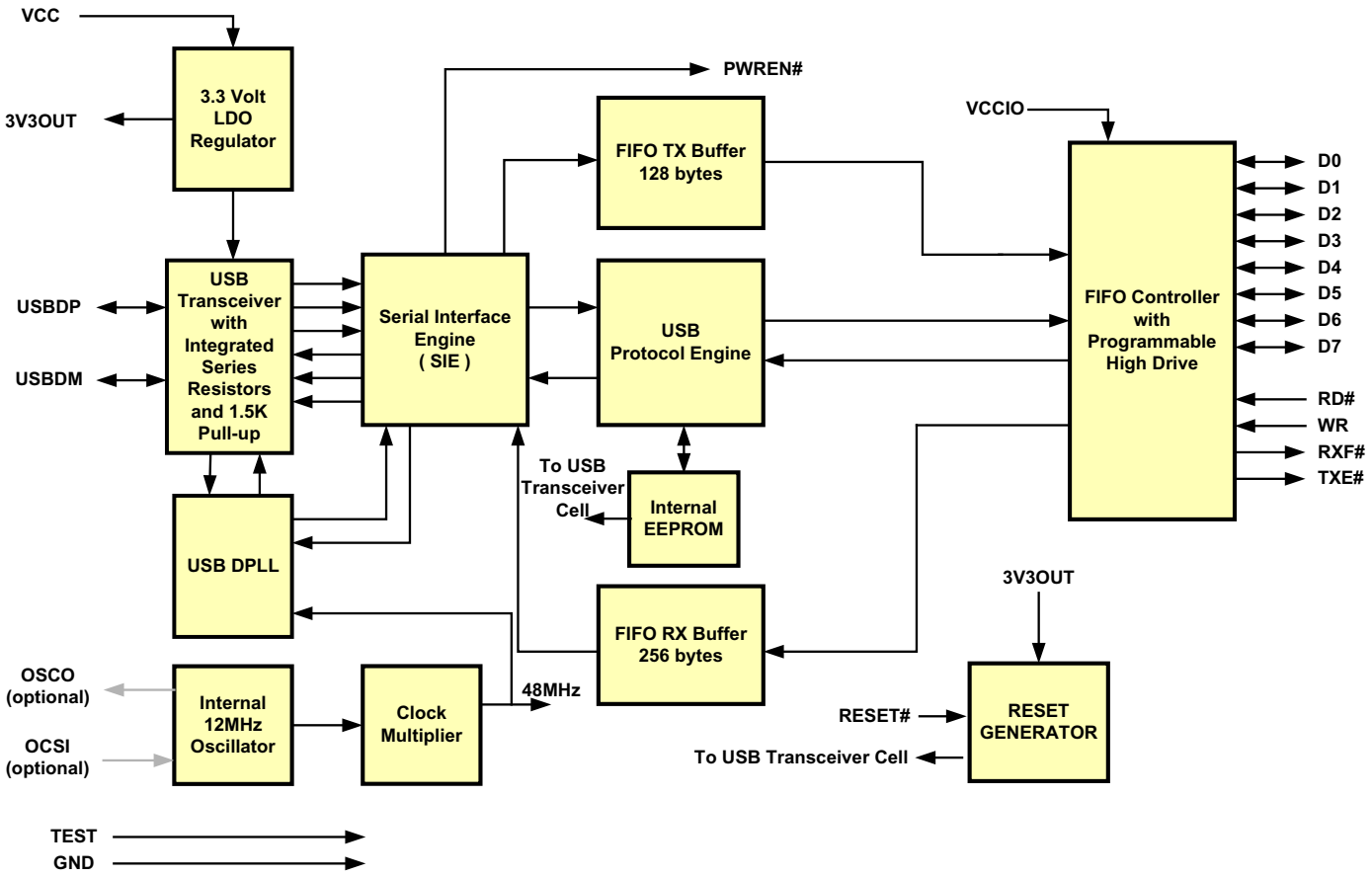

Figure 1 - FT245R Block Diagram

3.2 Functional Block Descriptions

3.3V LDO Regulator - The 3.3V LDO Regulator generates the 3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of this block is to power the USB Transceiver and the Reset Generator Cells, rather than to power external logic. However, external circuitry requiring 3.3V nominal at a current of around 50mA could also draw its power from the 3V3OUT pin if required.

USB Transceiver - The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3V level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection. This Cell also incorporates internal USB series resistors on the USB data lines, and a 1.5kΩ pull up resistor on USBDP.

USB DPLL - The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.

Internal 12MHz Oscillator - The Internal 12MHz Oscillator cell generates a 12MHz reference clock input to the x4 Clock multiplier. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and FIFO controller blocks

Clock Multiplier - The Clock Multiplier takes the 12MHz input from the Oscillator Cell and generates the 48MHz clock reference used for the USB DPLL block.

Serial Interface Engine (SIE) - The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 2.0 specification, it performs bit stuffing / un-stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

USB Protocol Engine - The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the FIFO.

FIFO TX Buffer (128 byte) - Data written into the FIFO using the WR pin is stored in the FIFO TX (transmit) Buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data In endpoint.

FIFO RX Buffer (256 byte) - Data sent from the USB host controller to the FIFO via the USB data Out endpoint is stored in the FIFO RX (receive) buffer and is removed from the buffer by reading the contents of the FIFO using the RD# pin.

FIFO Controller - The FIFO controller handles the transfer of data between the external FIFO interface pins (D0 - D7) and the FIFO transmit and receive buffers. A new feature, which is enabled in the internal EEPROM allows high signal drive strength on the FIFO parallel data bus and handshake control pins.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. A RESET# input is provided to allow other devices to reset the FT245R. RESET# can be tied to VCCIO or left unconnected, unless there is a requirement to reset the FT245R device from external logic or an external reset generator I.C.

Internal EEPROM - The internal EEPROM in the FT245R can be used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string, and various other USB configuration descriptors. The device is supplied with the internal EEPROM settings preprogrammed as described in Section 10.

4. Device Pin Out and Signal Descriptions

4.1 28-LD SSOP Package

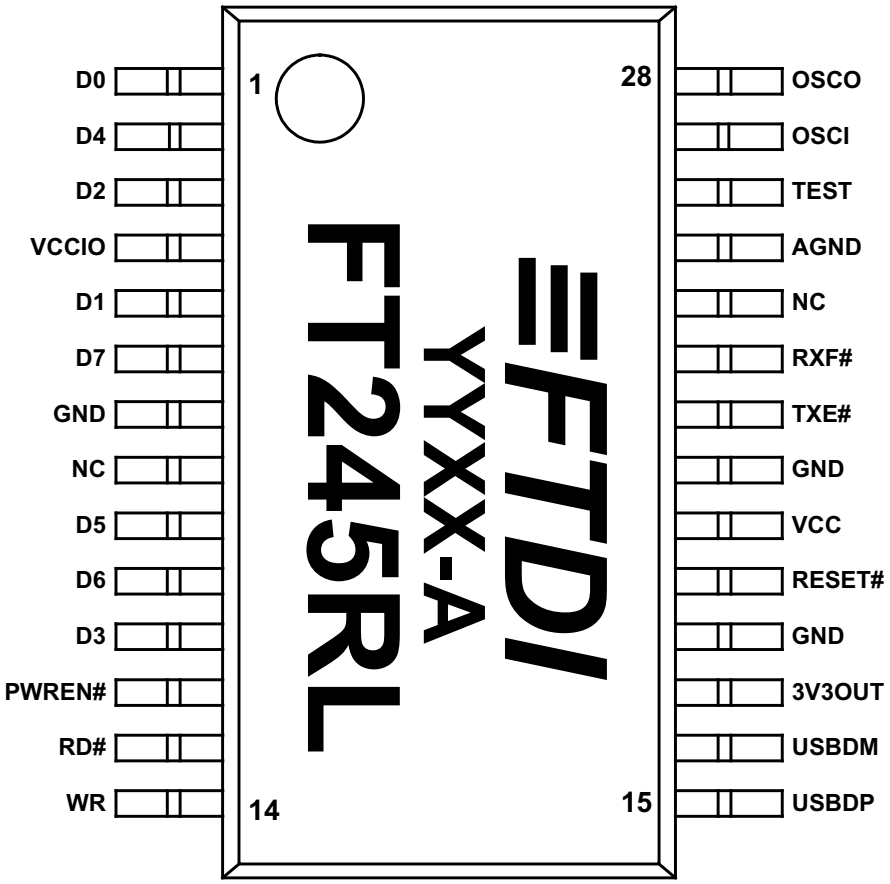

Figure 2 - 28 Pin SSOP Package Pin Out

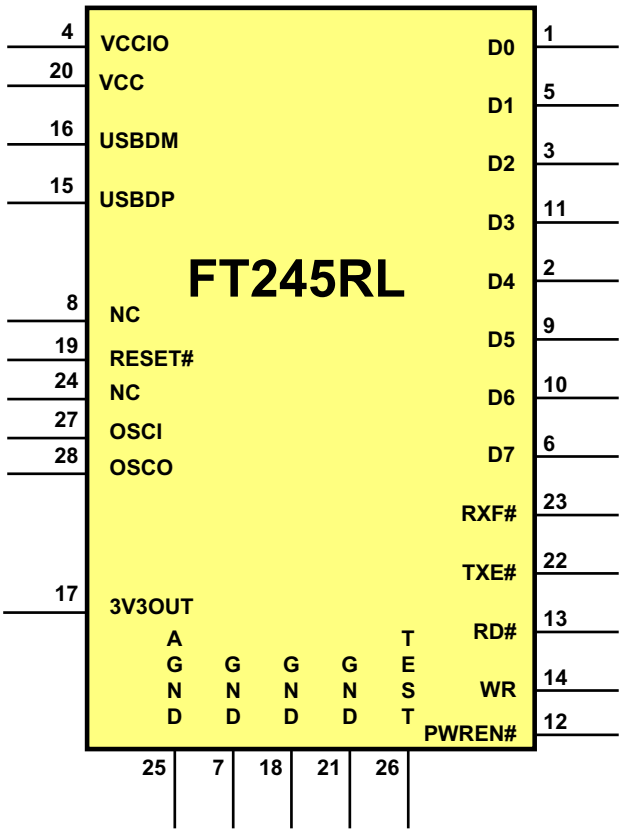

Figure 3 - 28 Pin SSOP Package Pin Out (Schematic Symbol)

4.2 SSOP-28 Package Signal Descriptions

Table 1 - SSOP Package Pin Out Description

Pin No.	Name	Type	Description
USB Interface Group			
15	USBDP	I/O	USB Data Signal Plus, incorporating internal series resistor and 1.5kΩ pull up resistor to 3.3V
16	USBDM	I/O	USB Data Signal Minus, incorporating internal series resistor.
Power and Ground Group			
4	VCCIO	PWR	+1.8V to +5.25V supply to the FIFO Interface and Control group pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect to 3V3OUT to drive out at 3.3V levels, or connect to VCC to drive out at 5V CMOS level. This pin can also be supplied with an external 1.8V - 2.8V supply in order to drive out at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to Vcc. This means that in bus powered designs a regulator which is supplied by the 5V on the USB bus should be used.
7, 18, 21	GND	PWR	Device ground supply pins
17	3V3OUT	Output	3.3V output from integrated L.D.O. regulator. This pin should be decoupled to ground using a 100nF capacitor. The prime purpose of this pin is to provide the internal 3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the FT245R's VCCIO pin.
20	VCC	PWR	3.3V to 5.25V supply to the device core.
25	AGND	PWR	Device analog ground supply for internal clock multiplier
Miscellaneous Signal Group			
8, 24	NC	NC	No internal connection.
19	RESET#	Input	Can be used by an external device to reset the FT245R. If not required can be left unconnected or pulled up to VCCIO.
26	TEST	Input	Puts the device into I.C. test mode. Must be grounded for normal operation.
27	OSCI	Input	Input to 12MHz Oscillator Cell. Optional - Can be left unconnected for normal operation. *
28	OSCO	Output	Output from 12MHz Oscillator Cell. Optional - Can be left unconnected for normal operation if internal oscillator is used.*
FIFO Interface and Control Group			
1	D0	I/O	FIFO Data Bus Bit 0**
2	D4	I/O	FIFO Data Bus Bit 4**
3	D2	I/O	FIFO Data Bus Bit 2**
5	D1	I/O	FIFO Data Bus Bit 1**
6	D7	I/O	FIFO Data Bus Bit 7**
9	D5	I/O	FIFO Data Bus Bit 5**
10	D6	I/O	FIFO Data Bus Bit 6**
11	D3	I/O	FIFO Data Bus Bit 3**
12	PWREN#	Output	Goes low after the device is configured by USB, then high during USB suspend. Can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# pin in this way.
13	RD#	Input	Enables the current FIFO data byte on D0...D7 when low. Fetched the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low. See Section 4.5 for timing diagram. **
14	WR	Input	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low. See Section 4.5 for timing diagram. **
22	TXE#	Output	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor. See Section 4.5 for timing diagram.
23	RXF#	Output	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high again. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor. See Section 4.5 for timing diagram. If the Remote Wakeup option is enabled in the internal EEPROM, during USB suspend mode (PWREN# = 1) RXF# becomes an input which can be used to wake up the USB host from suspend mode. Strobing the pin low will cause the device to request a resume on the USB bus.

*Contact FTDI Support for details of how to use an external crystal, ceramic resonator, or oscillator with the FT245R.

** When used in Input Mode, these pins are pulled to VCCIO via internal 200kΩ resistors. These can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting this option in the internal EEPROM.

4.3 QFN-32 Package

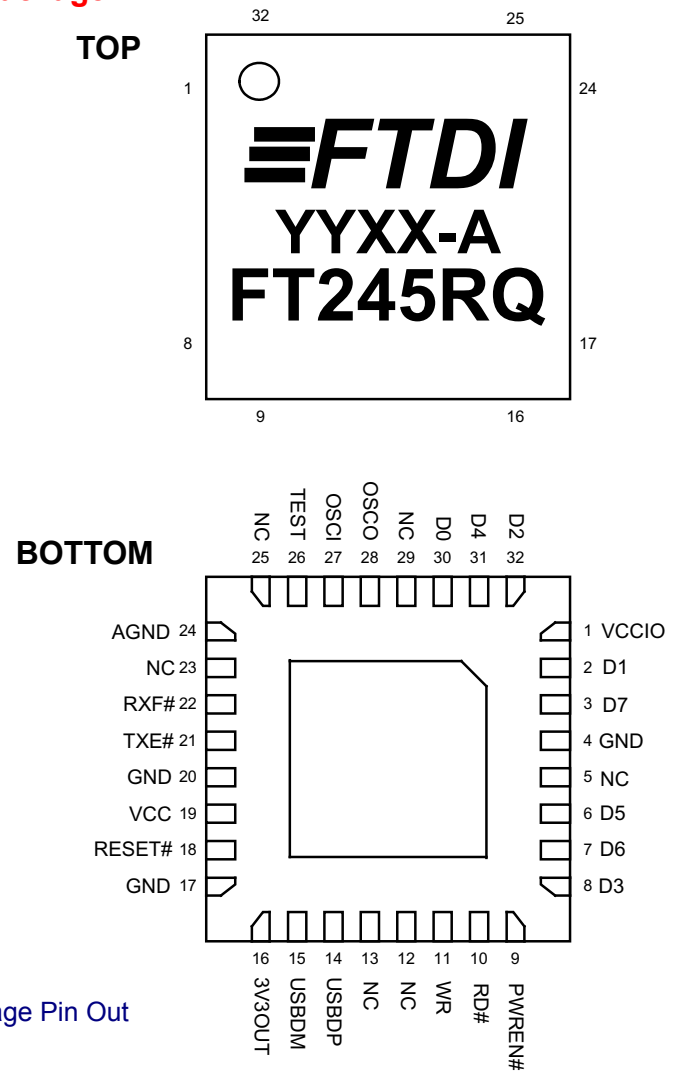

Figure 4 - QFN-32 Package Pin Out

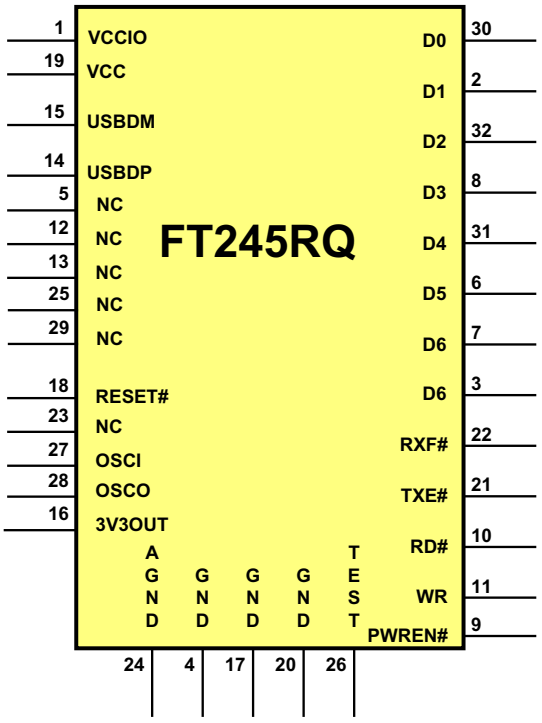

Figure 5 - QFN-32 Package Pin Out (Schematic Symbol)

4.4 QFN-32 Package Signal Descriptions

Table 2 - QFN Package Pin Out Description

Pin No.	Name	Type	Description
USB Interface Group			
14	USBDP	I/O	USB Data Signal Plus, incorporating internal series resistor and 1.5kΩ pull up resistor to 3.3V
15	USBDM	I/O	USB Data Signal Minus, incorporating internal series resistor.
Power and Ground Group			
1	VCCIO	PWR	+1.8V to +5.25V supply to FIFO Interface and Control group pins (2,3, 6, ...,11, 21, 22, 30,..32). In USB bus powered designs connect to 3V3OUT to drive out at 3.3V levels, or connect to VCC to drive out at 5V CMOS level. This pin can also be supplied with an external 1.8V - 2.8V supply in order to drive out at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to Vcc. This means that in bus powered designs a regulator which is supplied by the 5V on the USB bus should be used.
4, 17, 20	GND	PWR	Device ground supply pins
16	3V3OUT	Output	3.3V output from integrated L.D.O. regulator. This pin should be decoupled to ground using a 100nF capacitor. The prime purpose of this pin is to provide the internal 3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the FT245R's VCCIO pin.
19	VCC	PWR	3.3V to 5.25V supply to the device core.
24	AGND	PWR	Device analog ground supply for internal clock multiplier
Miscellaneous Signal Group			
5, 12, 13, 23, 25, 29	NC	NC	No internal connection.
18	RESET#	Input	Can be used by an external device to reset the FT245R. If not required can be left unconnected or pulled up to VCCIO.
26	TEST	Input	Puts the device into I.C. test mode. Must be grounded for normal operation.
27	OSCI	Input	Input to 12MHz Oscillator Cell. Optional - Can be left unconnected for normal operation. *
28	OSCO	Output	Output from 12MHz Oscillator Cell. Optional - Can be left unconnected for normal operation if internal oscillator is used. *
FIFO Interface and Control Group			
30	D0	I/O	FIFO Data Bus Bit 0**
31	D4	I/O	FIFO Data Bus Bit 4**
32	D2	I/O	FIFO Data Bus Bit 2**
2	D1	I/O	FIFO Data Bus Bit 1**
3	D7	I/O	FIFO Data Bus Bit 7**
6	D5	I/O	FIFO Data Bus Bit 5**
7	D6	I/O	FIFO Data Bus Bit 6**
8	D3	I/O	FIFO Data Bus Bit 3**
9	PWREN#	Output	Goes low after the device is configured by USB, then high during USB suspend. Can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# pin in this way.
10	RD#	Input	Enables the current FIFO data byte on D0...D7 when low. Fetched the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low. See Section 4.5 for timing diagram. **
11	WR	Input	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low. See Section 4.5 for timing diagram. **
21	TXE#	Output	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor. See Section 4.5 for timing diagram.
22	RXF#	Output	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high again. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor. See Section 4.5 for timing diagram. If the Remote Wakeup option is enabled in the internal EEPROM, during USB suspend mode (PWREN# = 1) RXF# becomes an input which can be used to wake up the host from suspend mode. Strobing the pin low will cause the device to request a resume on the USB bus.

*Contact FTDI Support for details of how to use an external crystal, ceramic resonator, or oscillator with the FT245R.

** When used in Input Mode, these pins are pulled to VCCIO via internal 200kΩ resistors. These can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting this option in the internal EEPROM.

4.5 FT245R FIFO Timing Diagrams

Figure 6 - FIFO Read Cycle

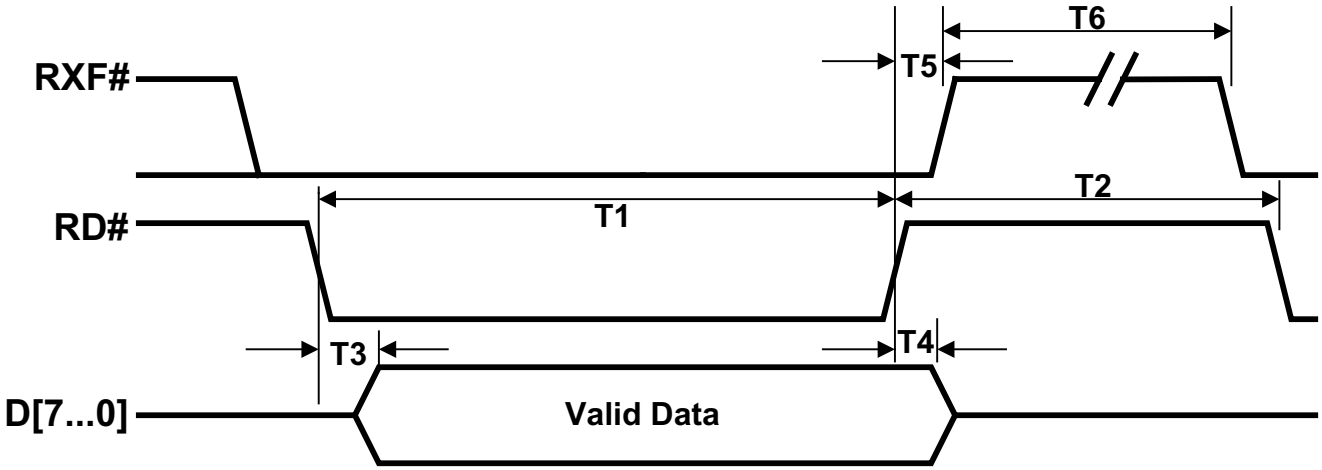

Table 3 - FIFO Read Cycle Timings

Time	Description	Min	Max	Unit
T1	RD Active Pulse Width	50		ns
T2	RD to RD Pre-Charge Time	50 + T6		ns
T3	RD Active to Valid Data*	20	50	ns
T4	Valid Data Hold Time from RD Inactive*	0		ns
T5	RD Inactive to RXF#	0	25	ns
T6	RXF Inactive After RD Cycle	80		ns

* Load = 30pF

Figure 7 - FIFO Write Cycle

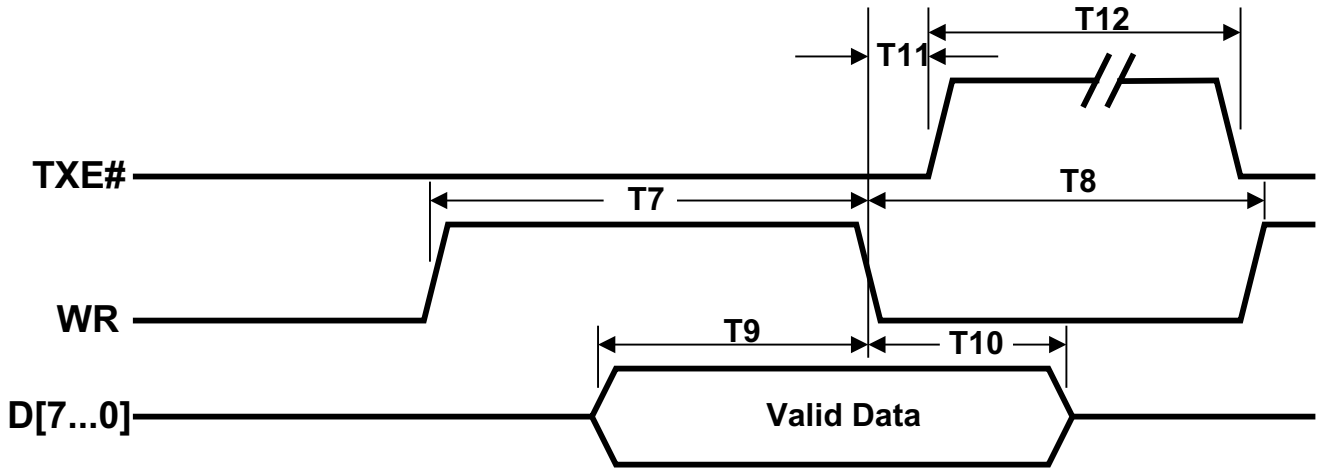

Table 4 - FIFO Write Cycle Timings

Time	Description	Min	Max	Unit
T7	WR Active Pulse Width	50		ns
T8	WR to RD Pre-Charge Time	50		ns
T9	Data Setup Time before WR Inactive	20		ns
T10	Data Hold Time from WR Inactive	0		ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE Inactive After WR Cycle	80		ns

5. Package Parameters

The FT245R is supplied in two different packages. The FT245RL is the SSOP-28 option and the FT245RQ is the QFN-32 package option. The solder reflow profile for both packages is described in Section 5.3.

5.1 SSOP-28 Package Dimensions

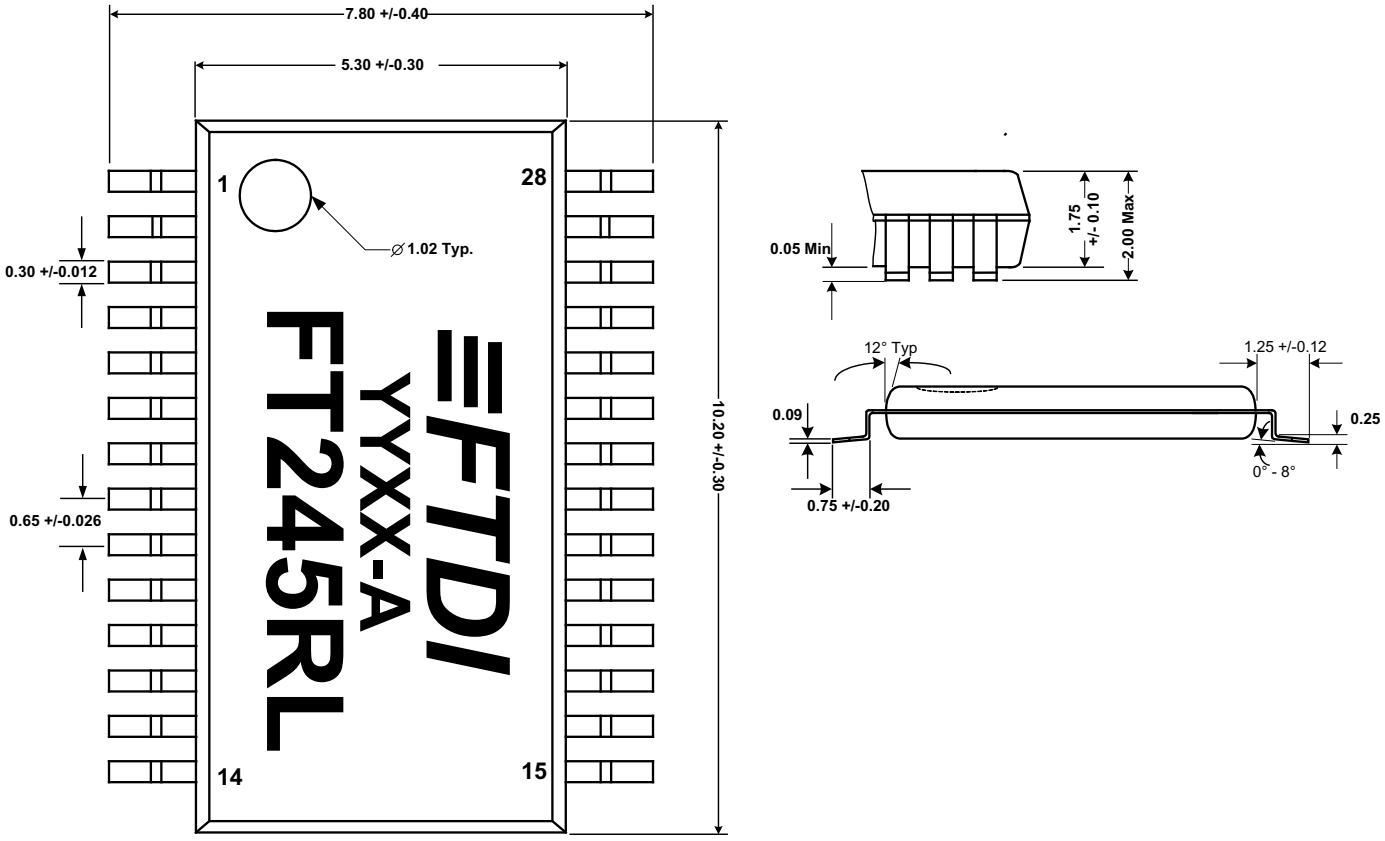

Figure 8 - SSOP-28 Package Dimensions

The FT245RL is supplied in a RoHS compliant 28 pin SSOP package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package has a 5.30mm x 10.20mm body (7.80mm x 10.20mm including pins). The pins are on a 0.65 mm pitch. The above mechanical drawing shows the SSOP-28 package – all dimensions are in millimetres.

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number.

5.2 QFN-32 Package Dimensions

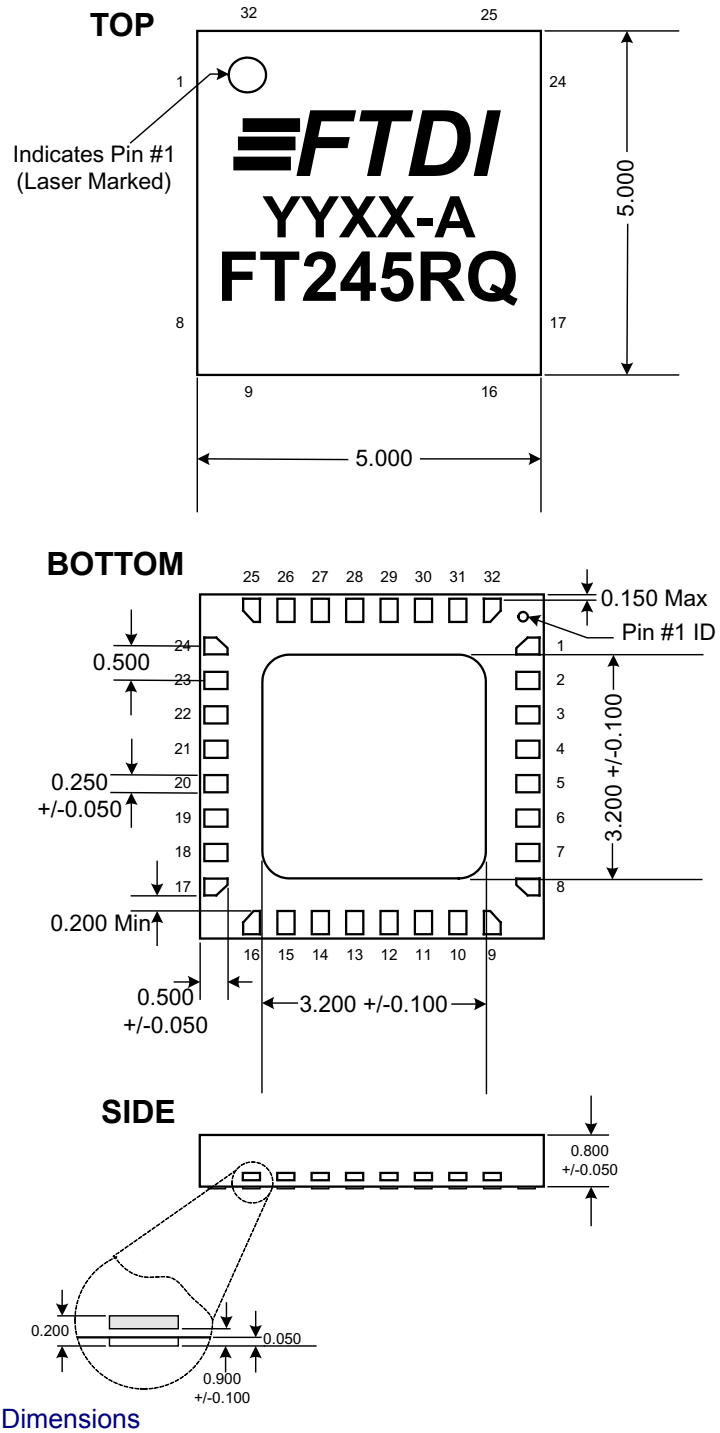

Figure 9 - QFN-32 Package Dimensions

The FT245RQ is supplied in a RoHS compliant leadless QFN-32 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package has a compact 5.00mm x 5.00mm body. The solder pads are on a 0.50mm pitch. The above mechanical drawing shows the QFN-32 package – all dimensions are in millimetres.

The centre pad on the base of the FT245RQ is not internally connected, and can be left unconnected, or connected to ground (recommended).

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number.

5.3 QFN-32 Package Typical Pad Layout

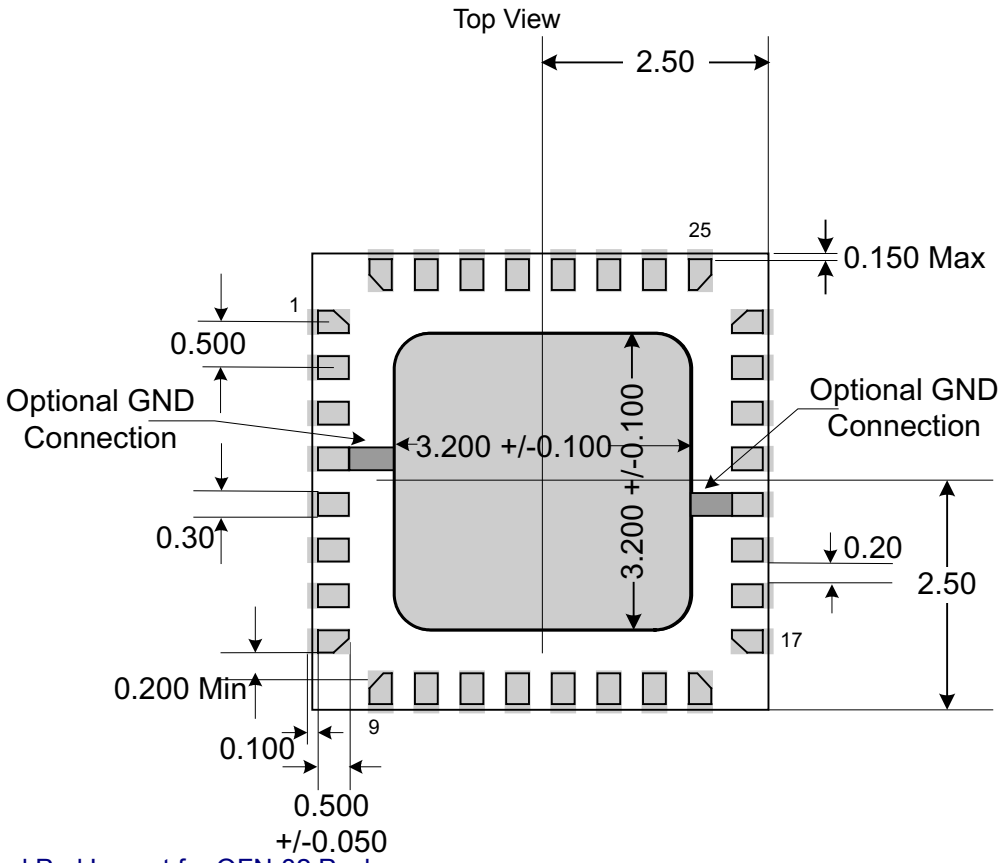

Figure 10 - Typical Pad Layout for QFN-32 Package

5.4 QFN-32 Package Typical Solder Paste Diagram

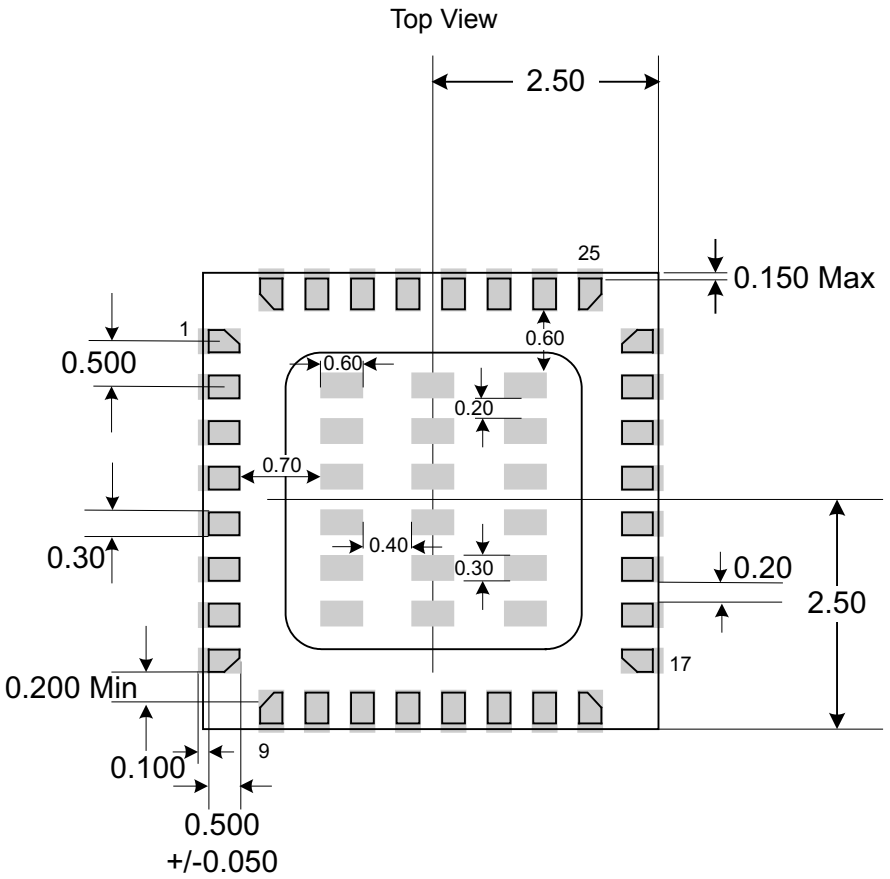

Figure 11 - Typical Solder Paste Diagram for QFN-32 Package

5.5 Solder Reflow Profile

The FT245R is supplied in Pb free 28 LD SSOP and QFN-32 packages. The recommended solder reflow profile for both package options is shown in Figure 12.

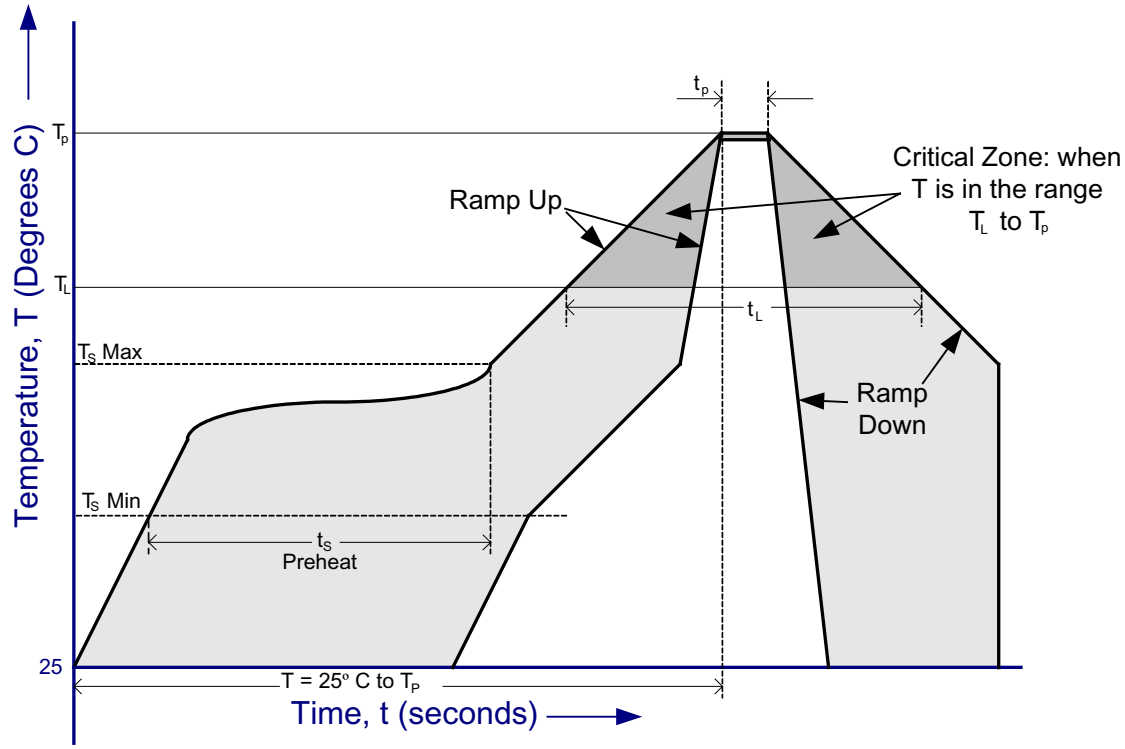

Figure 12 - FT245R Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 5. Values are shown for both a completely Pb free solder process (i.e. the FT245R is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT245R is used with non-Pb free solder).

Table 5 - Reflow Profile Parameter Values

Profile Feature	*Pb Free Solder Process*	*Non-Pb Free Solder Process*
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_S Min.) - Temperature Max (T_S Max.) - Time (t_S Min to t_S Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_P)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_P)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

6. Device Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT245R devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Table 6 - Absolute Maximum Ratings

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C.
Vcc Supply Voltage	-0.5 to +6.00	V
D.C. Input Voltage - USBDP and USBDM	-0.5 to +3.8	V
D.C. Input Voltage - High Impedance Bidirectionals	-0.5 to +(Vcc +0.5)	V
D.C. Input Voltage - All other Inputs	-0.5 to +(Vcc +0.5)	V
D.C. Output Current - Outputs	24	mA
DC Output Current - Low Impedance Bidirectionals	24	mA
Power Dissipation (Vcc = 5.25V)	500	mW

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 17 hours.

6.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Table 7 - Operating Voltage and Current

Parameter	Description	Min	Typ	Max	Units	Conditions
Vcc1	VCC Operating Supply Voltage	3.3	-	5.25	V	
Vcc2	VCCIO Operating Supply Voltage	1.8	-	5.25	V	
Icc1	Operating Supply Current	-	15	-	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	µA	USB Suspend

Table 8 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 5.0V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 9 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 3.3V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 10 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 2.8V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.1	2.6	3.1	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 11 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 5.0V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 12 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 3.3V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 13 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 2.8V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.1	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

**Inputs have an internal 200kΩ pull-up resistor to VCCIO.

Table 14 - RESET#, TEST Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

Table 15 - USB I/O Pin (USBDP, USBDM) Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15kΩ to GND (D-)
UVol	I/O Pins Static Output (Low)	0		0.3	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15kΩ to GND (D-)
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	26	29	44	Ohms	***

***Driver Output Impedance includes the internal USB series resistors on USBDP and USBDM pins.

6.3 EEPROM Reliability Characteristics

The internal 1024 Bit EEPROM has the following reliability characteristics-

Table 16 - EEPROM Characteristics

Parameter Description	Value	Unit
Data Retention	15	Years
Read / Write Cycles	100,000	Cycles

6.4 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics.

Table 17 - Internal Clock Characteristics

Parameter	Value			Unit
	Min	Typical	Max	
Frequency of Operation	11.98	12.00	12.02	MHz***
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

***Equivalent to +/-1667ppm.

Table 18 - OSCI, OSCO Pin Characteristics (Optional - Only applies if external Oscillator is used****)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.8	-	3.6	V	Fosc = 12MHz
Vol	Output Voltage Low	0.1	-	1.0	V	Fosc = 12MHz
Vin	Input Switching Threshold	1.8	2.5	3.2	V	

****When supplied the device is configured to use its internal clock oscillator. Users who wish to use an external oscillator or crystal should contact FTDI technical support.

7. Device Configurations

Please note that pin numbers on the FT245R chip in this section have deliberately been left out as they vary between the FT245RL and FT245RQ versions of the device. All of these configurations apply to both package options for the FT245R device. Please refer to Section 4 for the package option pin-out and signal descriptions.

7.1 Bus Powered Configuration

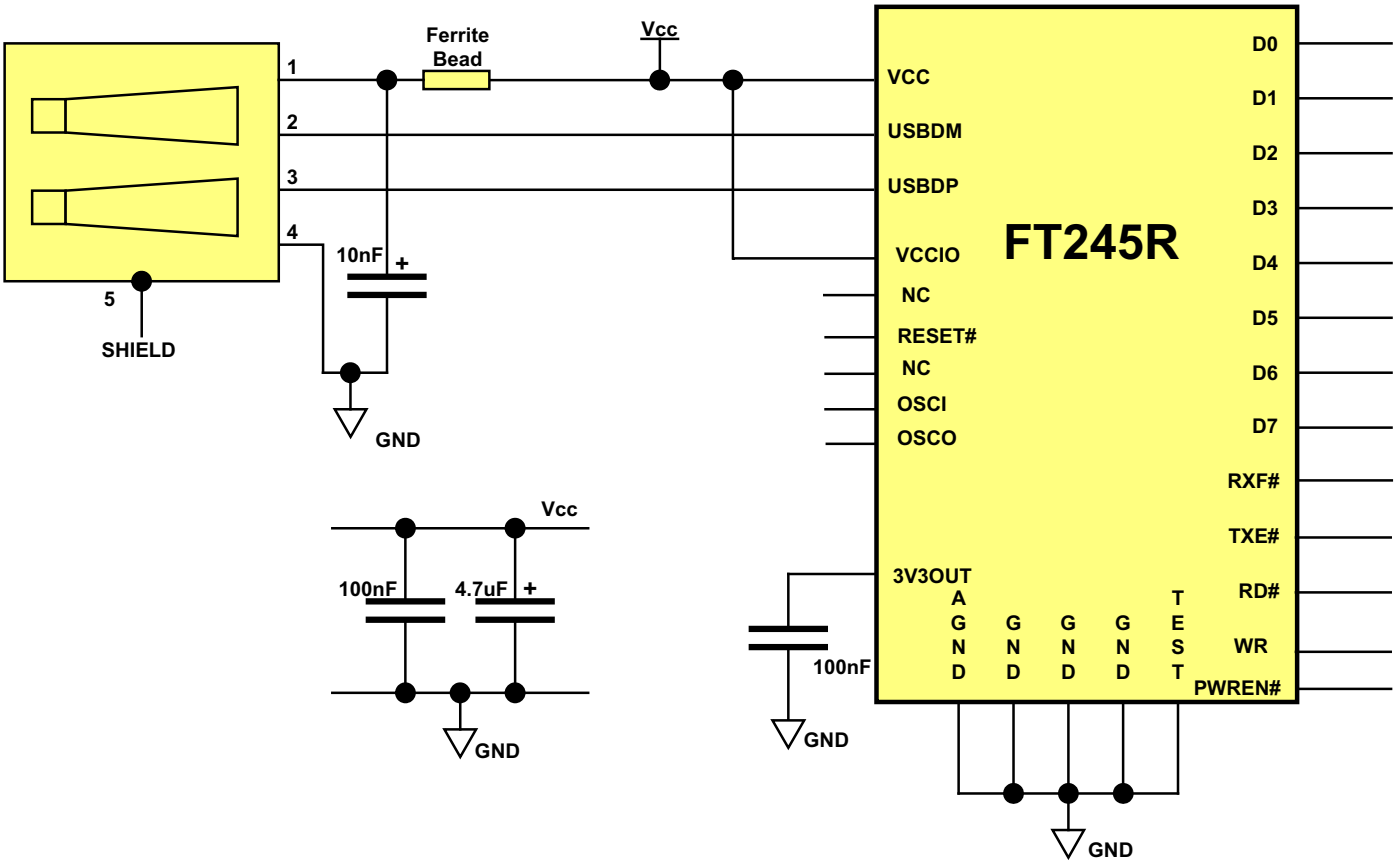

Figure 13 - Bus Powered Configuration

Figure 13 illustrates the FT245R in a typical USB bus powered design configuration. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

i) On plug-in to USB, the device must draw no more than 100mA.
ii) On USB Suspend the device must draw no more than 500µA.
iii) A Bus Powered High Power USB Device (one that draws more than 100mA) should use the PWREN# pin to keep the current below 100mA on plug-in and 500µA on USB suspend.
iv) A device that consumes more than 100mA can not be plugged into a USB Bus Powered Hub
v) No device can draw more that 500mA from the USB Bus.

The power descriptor in the internal EEPROM should be programmed to match the current draw of the device.
A Ferrite Bead is connected in series with USB power to prevent noise from the device and associated circuitry (EMI) being radiated down the USB cable to the Host. The value of the Ferrite Bead depends on the total current required by the circuit – a suitable range of Ferrite Beads is available from Steward (www.steward.com) for example Steward Part # MI0805K400R-00.

7.2 Self Powered Configuration

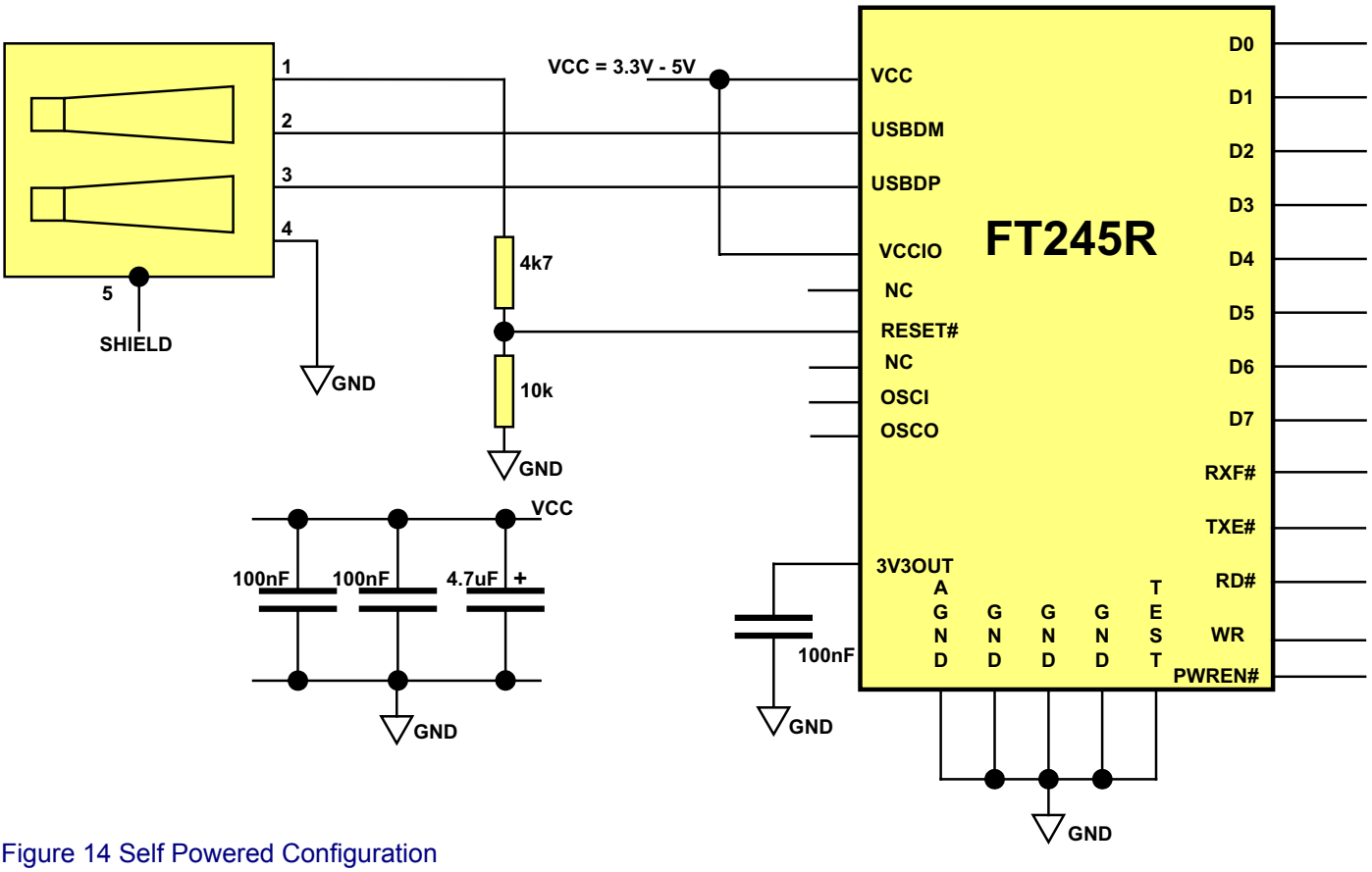

Figure 14 Self Powered Configuration

Figure 14 illustrates the FT245R in a typical USB self powered configuration. A USB Self Powered device gets its power from its own power supply and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows –

i) A Self Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.

ii) A Self Powered Device can use as much current as it likes during normal operation and USB suspend as it has its own power supply.

iii) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs

The power descriptor in the internal EEPROM should be programmed to a value of zero (self powered).

In order to meet requirement (i) the USB Bus Power is used to control the RESET# Pin of the FT245R device. When the USB Host or Hub is powered up the internal 1.5kΩ resistor on USBDP is pulled up to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, the internal 1.5kΩ resistor will not be pulled up to 3.3V, so no current will be forced down USBDP via the 1.5kΩ pull-up resistor when the host or hub is powered down. Failure to do this may cause some USB host or hub controllers to power up erratically.

Figure 10 illustrates a self powered design which has a 3.3V - 5V supply. A design which is interfacing to 2.8V - 1.8V logic would have a 2.8V - 1.8V supply to VCCIO, and a 3.3V - 5V supply to VCC

Note : When the FT245R is in reset, the FIFO interface and control pins all go tri-state. These pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

7.3 USB Bus Powered with Power Switching Configuration

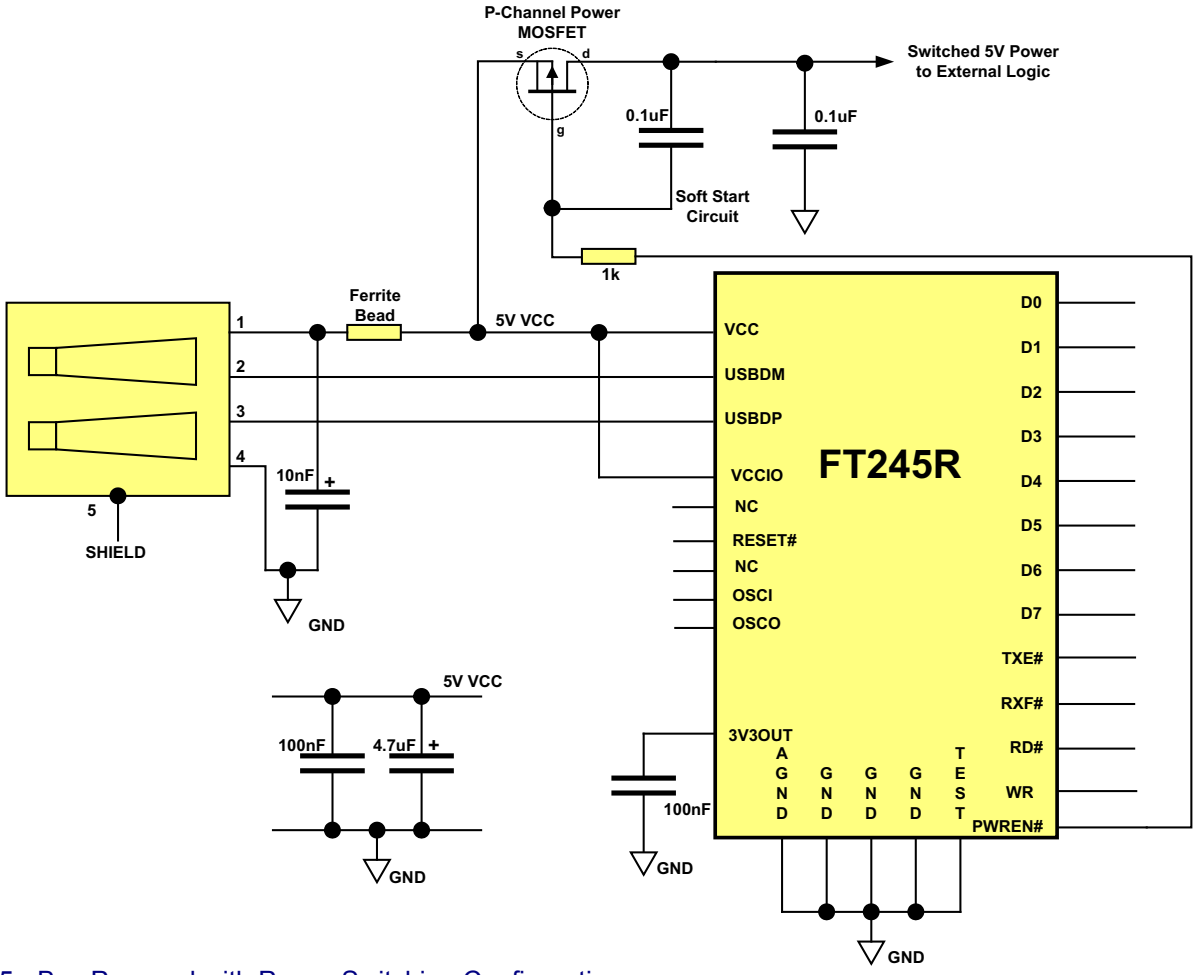

Figure 15 - Bus Powered with Power Switching Configuration

USB Bus powered circuits need to be able to power down in USB suspend mode in order to meet the <= 500µA total USB suspend current requirement (including external logic). Some external logic can power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way, the FT245R provides a simple but effective way of turning off power to external circuitry during USB suspend.

Figure 15 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device would be an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a “soft start” circuit consisting of a 1kΩ series resistor and a 0.1µF capacitor are used to limit the current surge when the MOSFET turns on. Without the soft start circuit there is a danger that the transient power surge of the MOSFET turning on will reset the FT245R, or the USB host / hub controller. The values used here allow attached circuitry to power up with a slew rate of ~12.5V per millisecond, in other words the output voltage will transition from GND to 5V in approximately 400 microseconds.

Alternatively, a dedicated power switch I.C. with inbuilt “soft-start” can be used instead of a MOSFET. A suitable power switch I.C. for such an application would be a Micrel (www.micrel.com) MIC2025-2BM or equivalent.

Please note the following points in connection with power controlled designs –

i) The logic to be controlled must have its own reset circuitry so that it will automatically reset itself when power is re-applied on coming out of suspend.
ii) Set the Pull-down on Suspend option in the internal EEPROM.
iii) The PWREN# pin should be used to switch the power to the external circuitry.
iv) For USB high-power bus powered device (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the device should be set in the max power field in the internal EEPROM. A high-power bus powered device must use this descriptor in the internal EEPROM to inform the system of its power requirements.
v) For 3.3V power controlled circuits the VCCIO pin must not be powered down with the external circuitry (the PWREN# signal gets its VCC supply from VCCIO). Either connect the power switch between the output of the 3.3V regulator and the external 3.3V logic or power VCCIO from the 3V3OUT pin of the FT245R.

7.4 USB Bus Powered with 3.3V / 5V Supply and Logic Drive / IO Supply Voltage

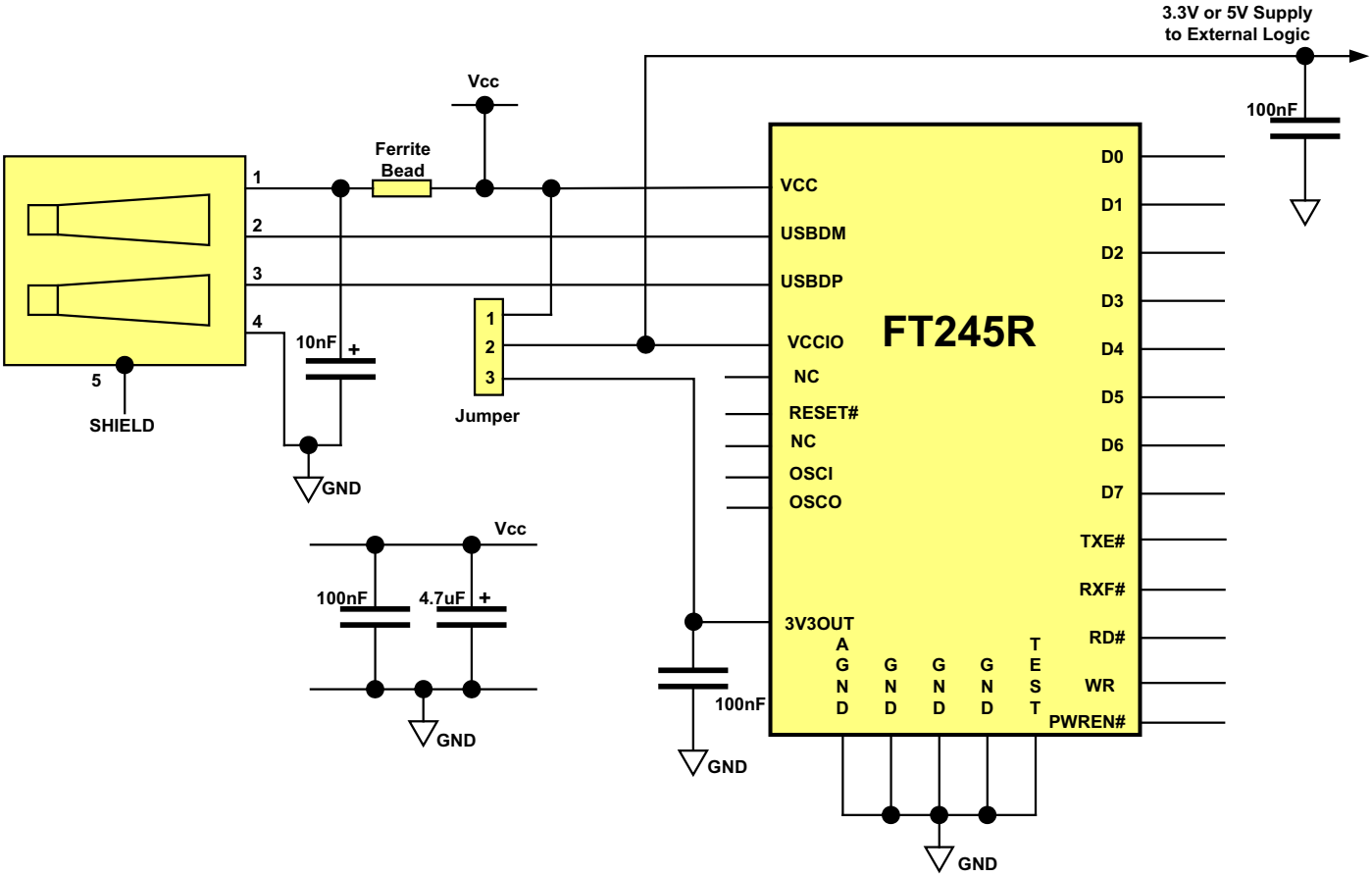

Figure 16 - Bus Powered with 3.3V / 5V Supply and Logic Drive

Figure 16 shows a configuration where a jumper switch is used to allow the FT245R to be interfaced with a 3.3V or 5V logic devices. The VCCIO pin is either supplied with 5V from the USB bus, or with 3.3V from the 3V3OUT pin. The supply to VCCIO is also used to supply external logic.

Please note the following in relation to bus powered designs of this type -

i) The PWREN# signal should be used to power down external logic during USB suspend mode, in order to comply with the limit of 500µA. If this is not possible, use the configuration shown in Section 7.3.
ii) The maximum current source from USB Bus during normal operation should not exceed 100mA, otherwise a bus powered design with power switching (Section 7.3) should be used.

Another possible configuration would be to use a discrete low dropout regulator which is supplied by the 5V on the USB bus to supply 2.8V - 1.8V to the VCCIO pin and to the external logic. VCC would be supplied with the 5V from the USB bus. With VCCIO connected to the output of the low dropout regulator, would in turn will cause the FT245R I/O pins to drive out at 2.8V - 1.8V logic levels.

For USB bus powered circuits some considerations have to be taken into account when selecting the regulator –

iii) The regulator must be capable of sustaining its output voltage with an input voltage of 4.35V. A Low Drop Out (L.D.O.) regulator must be selected.
iv) The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 500µA during USB suspend.

An example of a regulator family that meets these requirements is the MicroChip / Telcom TC55 Series of devices (www.microchip.com). These devices can supply up to 250mA current and have a quiescent current of under 1µA.

8. Example Interface Configurations

8.1 USB to MCU FIFO Interface Example

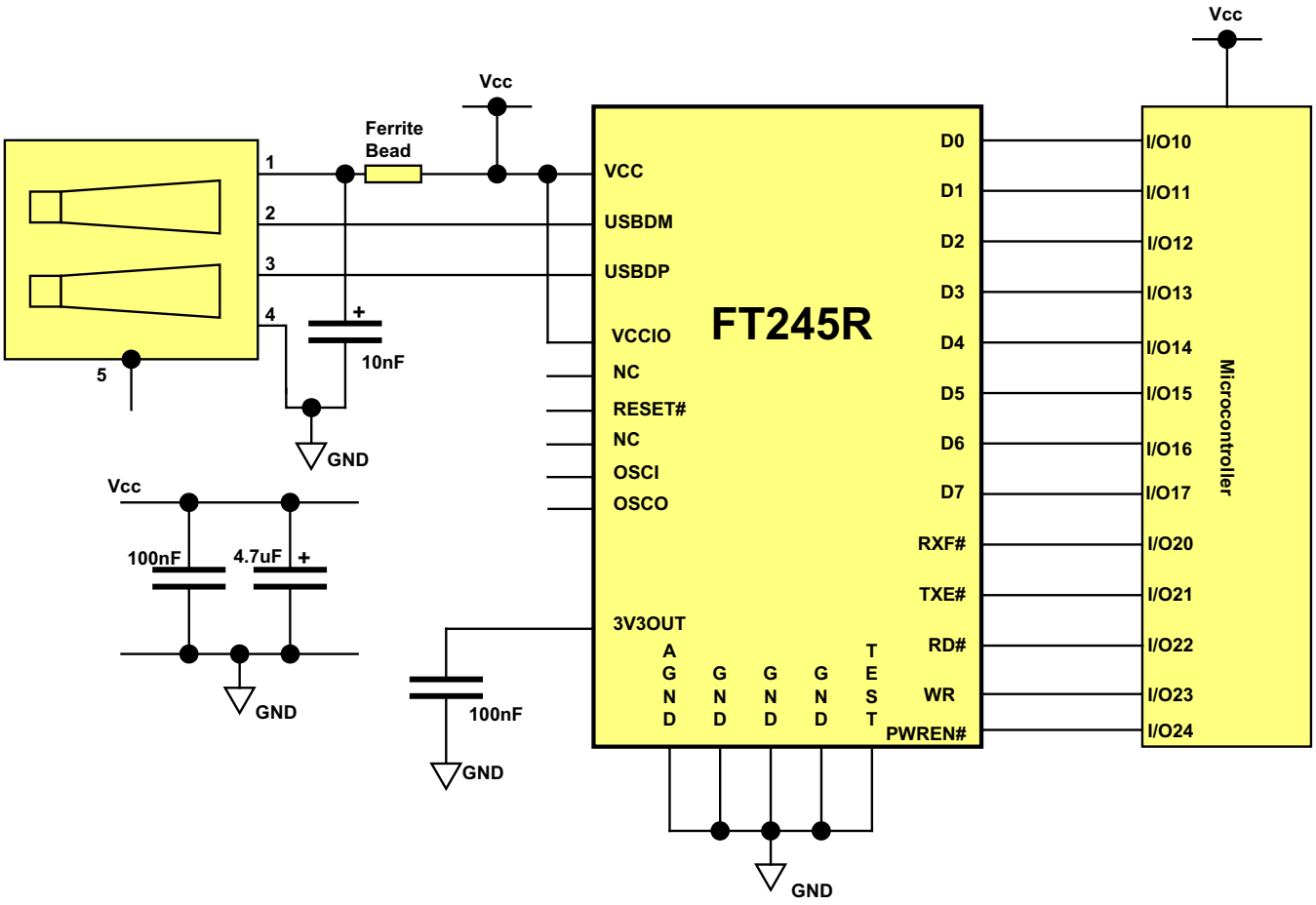

Figure 17 -Example USB to MCU FIFO Interface

Figure 17 illustrates a typical interfacing between the FT245R and a Microcontroller (MCU) FIFO interface. This example uses two I/O ports: one port (8 bits) to transfer data, and the other port (4 or 5 bits) to monitor the TXE# and RXF# status bits and generate the RD# and WR strobes to the FT245R, as required. Using PWREN# for this function is optional.

If the Remote Wakeup option is enabled in the internal EEPROM, during USB suspend mode RXF# becomes an input which can be used to wake up the USB host controller by strobing the pin low.

10. Internal EEPROM Configuration

Following a power-on reset or a USB reset the FT245R will scan its internal EEPROM and read the USB configuration descriptors stored there. The default values programmed into the internal EEPROM in a brand new device are defined in Table 19.

Table 19 - Default Internal EEPROM Configuration

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product ID (PID)	6001h	FTDI default PID (hex)
Serial Number Enabled?	Yes	
Serial Number	*See Note*	A unique serial number is generated and programmed into the EEPROM during device final test.
Pull Down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the FIFO interface lines when the power is shut off (PWREN# is high)
Manufacturer Name	FTDI	
Manufacturer ID	FT	Serial number prefix
Product Description	FT245R USB FIFO	
Max Bus Power Current	90mA	
Power Source	Bus Powered	
Device Type	FT245R	
USB Version	0200	Returns USB 2.0 device descriptor to the host. Note: The device is be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake up	Enabled	Taking RXF# low will wake up the USB host controller from suspend.
High Current I/Os	Disabled	Enables the high drive level on the FIFO data bus and control I/O pins
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.

The internal EEPROM in the FT245R can be programmed over USB using the utility program MPROG. MPROG can be downloaded from the FTDI website. Version 2.8a or later is required for the FT245R chip. Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. Contact FTDI support for this service.

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Version 0.94 - Revised Pre-release datasheet October 2005
Version 1.00 - Full datasheet released December 2005
Version 1.02 - Minor revisions to datasheet released 7th December 2005
Version 1.03 - Manufacturer ID added to default EEPROM data January 2006
Version 1.04 - 9th January 2006 Buffer sizes added.
Version 1.05 - 30th January 2006 QFN-32 Package pad layout and solder paste diagrams added.

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